Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC)

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I. Introduction

In Voltage Regulation Module (VRM) applications it is well known that the main driver in designing the output filter stage is the output impedance of the system due to the strict specifications imposed by the load. Therefore, the ongoing research trend is directed to improve the dynamic response of the VRM while reducing the size of the output capacitor by means of improving the controller [1]-[5] or by introducing an additional energy path to compensate the charge perturbation in the output capacitor [6]-[16].

Increasing the bandwidth of the classical regulator may lead to system instability due to the regulator component tolerances, temperature variations both of the converter and regulator, aging effects, as well the parasitics. In order to achieve higher robustness of the control, integration of low bandwidth linear loop and fast nonlinear loop may be applied. The well-known nonlinear V2 control is presented in [1]-[2], but it relies on sensing the output voltage ripple, which is very small compared to the DC value of the output voltage. Control techniques presented in [3]-[5] reduce the transient time utilizing the capacitor current which contains the information of the load behavior, thus reducing the response time of the control. The output capacitor current measurement is based on the noninvasive current sensor presented in [17]. These solutions can be applied on the fast Buck converter with high switching frequency. However, by increasing the switching frequency, the switching loses are increased as well. On the other hand, the second possibility is to introduce another energy path to compensate the charge unbalance of the output capacitor [6]-[16], thus reducing the transient time and the output voltage overshoot/undershoot. Most of the currently proposed solutions rely on the charge-balance control techniques [6]-[12] presenting inherent limitations, resulting that the system is operating in open loop during the transients, thus their performance will be degraded under other types of load perturbations than a step function. Solutions [13]-[16] are utilizing an additional energy path by injecting necessary current that compensates the capacitor current and prevents further output voltage deviation. The biggest limitation of all presented solutions is that they are developed for a Single Phase Buck converter with Voltage Mode Control (VMC), while in the VRM applications, due to the high output currents, the system is usually implemented as a Multiphase Buck Converter with Peak Current Mode Control (PCMC).

The Output Impedance Correction Circuit (OICC) concept has been presented in [18]. The solution utilizes an additional energy path, provided by the Output Impedance Correction Circuit (OICC), so that the auxiliary current, injected/extracted trough this path is controlled to have n-1 times higher value than the output capacitor current with appropriate directions. In order to measure the output capacitor current, noninvasive current sensor from [17] is used. This work expands the OICC concept to a Multiphase Buck Converter system while comparing the proposed solution with the system that has n times bigger output capacitor. Furthermore, the OICC is implemented as a Synchronous Buck Converter with PCMC, thus improving the efficiency of the system compared to the

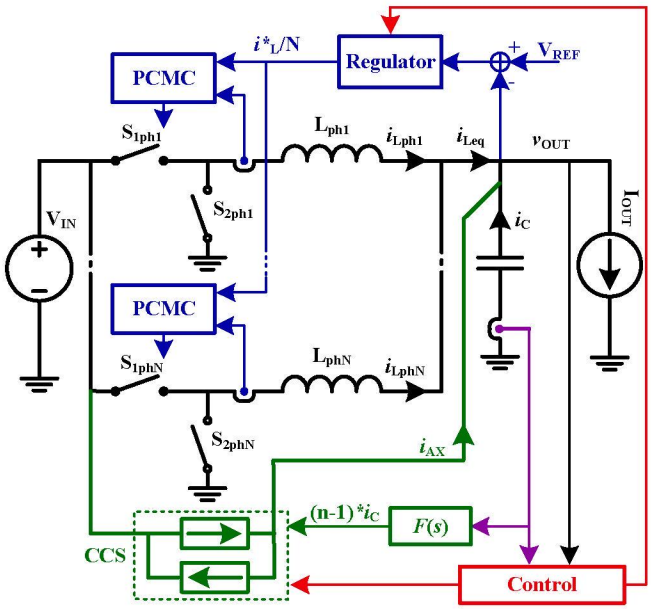

Figure 1. Multiphase Buck Converter with the OICC - Buck converter (black), the current measurement, driving signal generation and the regulator (blue), non-invasive current sensor (purple), the OICC (green) and system control (red).

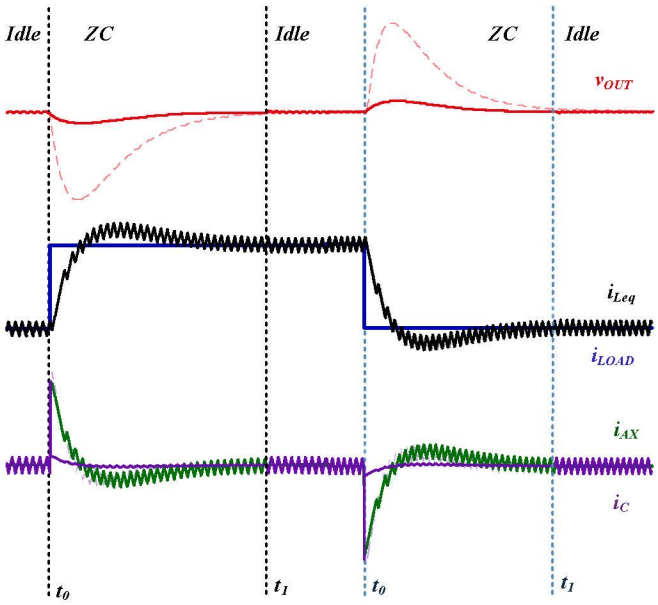

Figure 2. Ideal system waveforms: load step transitions with (solid) and without (dotted) the OICC.

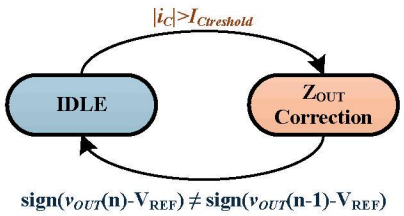

Figure 3. The State machine of the system control.

solution with Linear Regulator (LR) implementation, presented in [18].

II. The Output Impedance Correction Circuit – Ideal Operation

A Multiphase Buck Converter with Peak Current Mode Control (PCMC) and with the OICC is shown in Fig. 1. As explained in [18], the system utilizes the OICC in a manner that the OICC injects/extracts a current in the output node that is n-1 times bigger than the output capacitor current with corresponding directions. This behavior of the OICC virtually increases the output capacitance n times during the transients, thus reducing the output impedance by the same factor. The system is composed of the Multiphase Buck converter (black) with a slow regulator (blue) that can be dynamically modified, the OICC (green - power stage, purple - current measurement) behaving like a controlled current source and the system control (red). The control block allows the OICC to inject/extract the current only in the certain states of the transient routine. At the same time, in order to maintain the stability of the system, the control modifies the main converter regulator.

During the steady-state, the OICC is inactive; all energy is transferred trough the Multiphase Buck converter and it is behaving like a voltage source while the system control is observing the output capacitor current in order to initialize the transient routine when a load step occurs. In this manner, by observing the output capacitor current, the system reacts nearly instantaneously to a load perturbation, since the output capacitor current is the fastest variable in the system that sees this perturbation. In Fig. 2 the ideal transition routine behavior is presented. The waveforms of the system variables with OICC are presented as a solid line and without the OICC are presented as a dotted line. In the steady state operation, the OICC is turned off and the small load variations are regulated by the low bandwidth regulator. When the load step occurs, the OICC is activated and the output impedance correction starts. The system controller, implemented as a state machine in Fig. 3 is triggered by the output capacitor current in the time instant t_0 and the system goes to the Z_{OUT} *Correction* state (ZC in Fig. 2). In this state, the OICC is providing n-1 times more current than the output capacitor, thus reducing the amount of the charge extracted/injected from/to the output capacitor. As a result, the voltage perturbation is smaller. In order to end the Z_{OUT} *Correction* state, the system controller is observing the output voltage error signal. When the error signal sign is changed in t_1, the output voltage is equal or close to the reference voltage and that event triggers the system controller which returns the system back to the *Idle* state.

During the *Idle* state, the output capacitance is C, but during the Z_{OUT} *Correction* state, the equivalent capacitance in ideal case is n·C. This affects the PCMC Multiphase Buck converter averaged model and, therefore, the stability requirements related to the regulator modification addressed in [18] need to be satisfied.

III. Synchronous PCMC Buck OICC Implementation

The OICC implementation is presented in Fig.4. The OICC subsystem is composed of non-invasive current sensor (purple) designed by applying the impedance matching

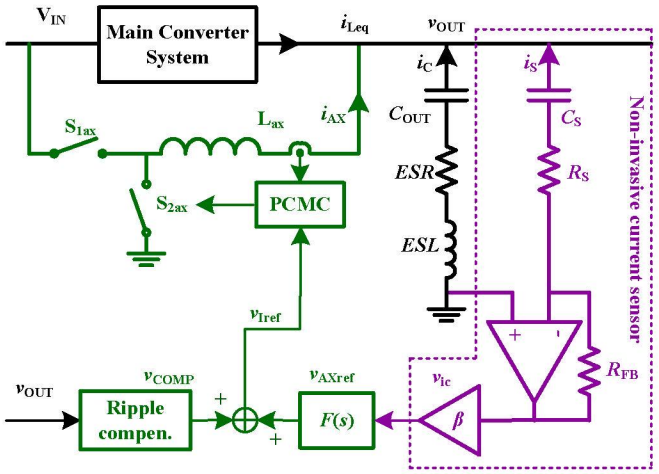

Figure 4. Implementation of the OICC – Synchronous Buck converter with PCMC, auxiliary reference generator and current ripple compensation (green), non-invasive current sensor (purple) and the main power stage (black).

procedure presented in [17], the auxiliary current reference generator, the current ripple compensation block and High-switching frequency Synchronous Buck converter with PCMC that operates as a controlled current source (CCS), shown in Fig. 1. When the OICC is active, the CCS is injecting an auxiliary current i_{AX} at the output node composed of the mean value given by the auxiliary current reference generator v_{AXref} and the high frequency component generated by the Buck converter. Since the Buck converter is PCMC controlled, an offset between the current reference v_{Iref} and the mean value of the auxiliary current i_{AX} exists due to the current ripple, the compensation ramp and due to the turn on/off delays of the PCMC modulator. Therefore, the current ripple compensation block is employed to compensate the difference by adding v_{COMP} to the auxiliary current reference voltage v_{AXref}, thus ensuring that the mean value of the auxiliary current i_{AX} equals to the auxiliary current reference voltage v_{AXref}.

Fig. 5 shows PCMC waveforms and it can be seen that, due to the type of the modulation, the mean value of the auxiliary current i_{AX} is not equal to the current reference v_{Iref}. Depending on the slope of the compensation ramp m_C, turn-on and turn-off delay ($t_{HI\uparrow}$ and $t_{HI\downarrow}$) as well on the comparator delay t_{COMP}, the difference between the current reference v_{Iref} and the mean value of the auxiliary current i_{AX}, which needs to be compensated by the compensation block v_{COMP}, can be derived and it is

$$v_{COMP} = v_{Iref} - i_{AX} = \frac{v_{OUT}}{2Lf_{SW}} - \frac{v_{OUT}^2}{2Lf_{SW}v_{IN}} + \frac{m_C}{f_{SW}}\frac{v_{OUT}}{v_{IN}} + m_C\left(t_{HI\uparrow} - t_{HI\downarrow} - t_{COMP}\right) - \left(v_{IN} - v_{OUT}\right)\frac{t_{HI\downarrow} + t_{COMP}}{L} \quad (1)$$

Linearizing (1) in operating point defined with V_{IN} and V_{OUT}, linear dependence of the compensating voltage v_{COMP} on input variables v_{IN} and v_{OUT} is obtained and given by

$$v_{COMP} = V_{COMP} + k_1\left(v_{OUT} - V_{OUT}\right) + k_2\left(v_{IN} - V_{IN}\right), \quad (2)$$

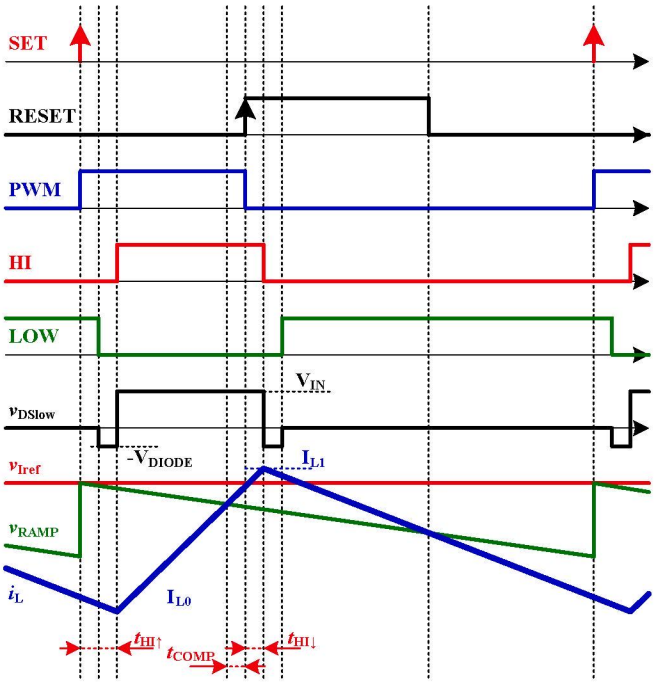

Figure 5. PCMC wavefoarms with delays.

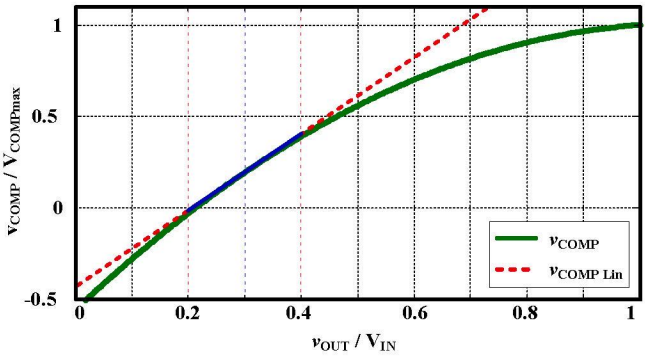

Figure 6. Normalized compensation voltage: dependance on the normalized output voltage (green), linearization at the operating point (red-dotted) and part of the linearized function in the region of interest (blue).

where V_{COMP} is DC value of the v_{COMP} and k_1 and k_2 slopes of the plane defined with (2) and given by

$$k_1 = \frac{1}{2Lf_{SW}} - \frac{V_{OUT}}{Lf_{SW}V_{IN}} + \frac{m_C}{f_{SW}V_{IN}} + \frac{t_{HI\downarrow} + t_{COMP}}{L}$$
$$k_2 = \frac{V_{OUT}^2}{2Lf_{SW}V_{IN}^2} - \frac{m_C}{f_{SW}}\frac{V_{OUT}}{V_{IN}^2} - \frac{t_{HI\downarrow} + t_{COMP}}{L} \quad (3)$$

Additionally, an assumption that the input voltage v_{IN} is constant leads to further simplification of (3) which leads to

$$v_{COMP} = V_{COMP} + k_1\left(v_{OUT} - V_{OUT}\right). \quad (4)$$

Limitation of the bandwidth of v_{OUT} needs to be included in order to minimize the influence of the switching ripple of both the main system and the OICC. The current ripple

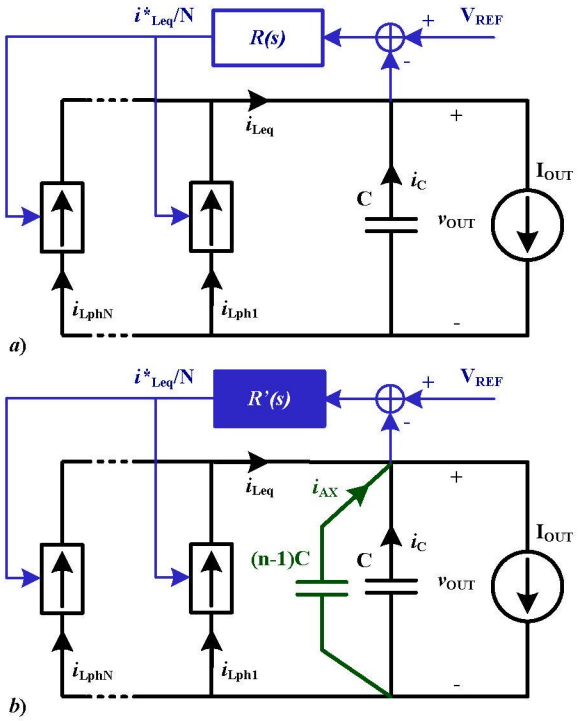

Figure 7. Averaged models of the system during *a*) the *Idle* state and *b*) Z_{OUT} *Correction* state.

compensation block, defined with (4), has been implemented as a linear amplifier with limited bandwidth. The bandwidth is the same as the closed-loop bandwidth of the main converter system in order to follow the dynamic of the output voltage.

Normalized compensation voltage v_{COMP} is shown in Fig.6. For the presented case, the delays are selected to be realistic for high-frequency application with discrete implementation ($t_{HI\uparrow}$ is $0.08T_{SW}$, $t_{HI\downarrow}$ is $0.1T_{SW}$ and t_{COMP} is $0.07T_{SW}$). It can be seen from Fig. 6 that a relatively good overlapping of the simplification (red) defined with (4) and the real dependency (green) defined with (1) can be obtained.

In order to ensure the large signal stability of the OICC subsystem, the high-frequency component of the auxiliary current, which is seen in the capacitor current measurement (v_{ic}), needs to be filtered by the auxiliary current reference generator. The auxiliary current reference generator transfer function is given by

$$F(s)=\frac{v_{AXref}(s)}{v_{ic}(s)}=\frac{n-1}{1+\dfrac{s}{2\pi f_{OICCc}}} \qquad (5)$$

where n is the output capacitor multiplication factor and f_{OICCc} is the frequency up to which the OICC has constant gain n-1. By implementing (5), the OICC system corrects the output impedance up to f_{OICCc}, which needs to be higher frequency than the closed loop bandwidth of the main converter system in order to minimize the influence of the pole in (5) on the closed-loop gain. In that case, the OICC is behaving as n-1

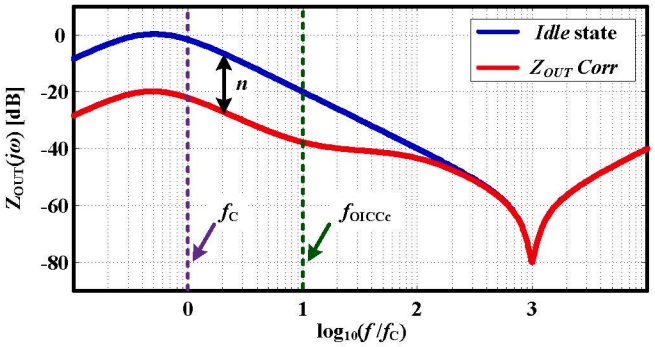

Figure 8. The output impedance of the system in *Idle* (blue) and Z_{OUT} *Correction* (red) state

times bigger capacitor in low frequency part of the spectrum, thus the linearized model of the whole system can be simplified and it is presented in Fig. 7.

The impedance seen at the output node when the OICC is active is

$$Z_{Cout}^{EQ}=\frac{Z_{Cout}}{1+F(s)}\xrightarrow{f<f_{OICCc}}Z_{Cout}^{EQ}=\frac{Z_{Cout}}{n}, \qquad (6)$$

where Z_{Cout} is the impedance of the output capacitor and the open-loop impedance of the system during the *Idle* state.

According to [18], the regulator needs to be modified in order to maintain the same closed-loop gain characteristics by applying

$$R'(s)=nR(s), \qquad (7)$$

where R(s) and R'(s) are the regulator transfer functions for the system operating in *Idle* and Z_{OUT} *Correction* states, respectively.

The closed-loop impedance of the system during the *Idle* state is given by

$$Z_{OUT}(s)=\frac{Z_{Cout}}{1+L(s)}, \qquad (8)$$

where, $L(s)$ is closed loop gain in both states. The output impedance with OICC is

$$Z'_{OUT}(s)=\frac{Z_{Cout}^{EQ}}{1+L(s)}\xrightarrow{f<f_{OICCc}}Z'_{OUT}(s)=\frac{Z_{OUT}(s)}{n} \qquad (10)$$

The output impedance of the system in both *Idle* and Z_{OUT} *Correction* state is plotted in Fig. 8. The reduction of the output impedance of the system in Z_{OUT} *Correction* state by factor n is achieved up to the OICC corner frequency f_{OICCc}.

IV. Simulations and Experimental Results

In order to demonstrate and compare simulated and the real dynamic behavior, two prototypes (A and B) are designed and built and the specifications are presented in Table I. The

first prototype, Prototype A, has the output capacitor of 140 µF and it utilizes the OICC in order to improve the dynamic behavior. The OICC has been implemented as Synchronous Buck converter with PCMC which has multiplication factor of 15 and the OICC corner frequency f_{OICCc} at 50 kHz. On the other hand, Prototype B has been designed to have the same power stage as the Prototype A with the difference that, instead of using the OICC, it has 15 times bigger output capacitor which is implemented with 2 OSCON capacitor of 570 µF, 8 ceramic capacitors of 100 µF and 2 ceramic capacitors of 47 µF.

System simulations under the resistive load step of 8.2 A (SR+ = 11 A/µs and SR- = -270 A/µs) are performed for Prototype A system both with and without the OICC and on the Prototype B system. The corresponding waveforms for the load step-up are presented in Fig. 9, Fig. 10 and Fig. 11, respectively. It can be seen that Prototype A with the OICC has similar behavior as Prototype B, having the undershoot of ~30 mV and the transient of ~100 µs, with the difference that the high frequency ripple at the output voltage exists due to the switching of the auxiliary Buck. In addition, Prototype A with the OICC enters in an additional settling transient due to the regulator modification and has a small deviation of 20 mV. Furthermore, the Prototype A with the OICC has 12 times smaller deviation compared to the case when the OICC is inactive (375 mV).

In order to verify the assumptions made in the simulations, the same experiment has been performed for both prototypes under the same conditions and the waveforms are presented in Fig. 12 and Fig. 13, for Prototype A with and without the OICC, respectively, and in Fig. 14 for Prototype B. It can be observed that the results are in a good agreement with the simulations for both prototypes (Fig.9, Fig. 10 and Fig. 11).

Furthermore, Fig. 12 shows how auxiliary current is injected at the output node only during the transient and how the high frequency ripple is degrading the output voltage, which can be improved by utilizing better PCB-layout

TABLE I. THE CONVERTER SPECIFICATION

		Prototype A	Prototype B
Main Conv. (2 Phase PCMC)	V_{IN}	5 V	5 V
	V_{OUT}	1.5 V	1.5 V
	f_{SW} per Phase	150 kHz	150 kHz
	L per Phase	2 µH	2 µH
	C_{OUT}	**3 x 47 µF** (ESL = ~4 nH, ESR = ~7 mΩ);	**2x 560 µF** (ESL = ~9 nH, ESR = ~18 mΩ); **8x 100 µF** (ESL = ~2 nH, ESR = ~5 mΩ); **2x 47 µF** (ESL = ~1 nH, ESR = ~5 mΩ);
	MOSFETs	SI4866BDY	SI4866BDY
	Driver	ISL6605	ISL6605
Auxiliary Conv.	f_{SW}	5 MHz	-
	L	100 nH	-
	n	15	-
	f_{OICCc}	50 kHz	-
	MOSFETs	FDMS7620S	-
	Driver	ISL6605	-

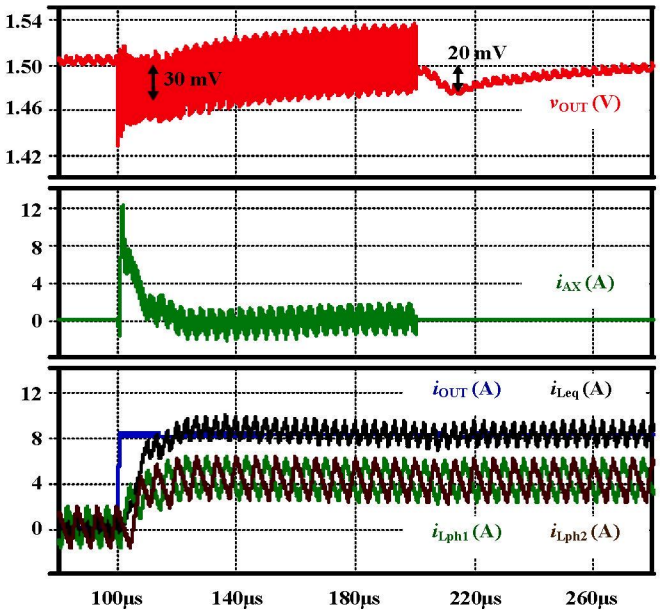

Figure 9. Simulation results – the load step-up Prototype A with the OICC: C_{OUT} 140µF.

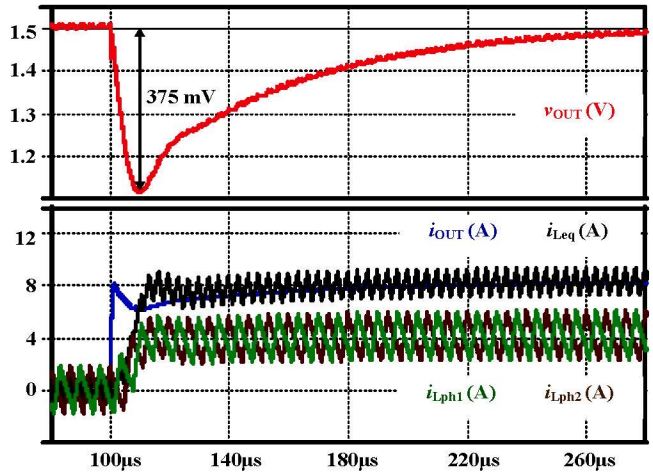

Figure 10. Simulation results – the load step-up Prototype A without the OICC: C_{OUT} 140µF.

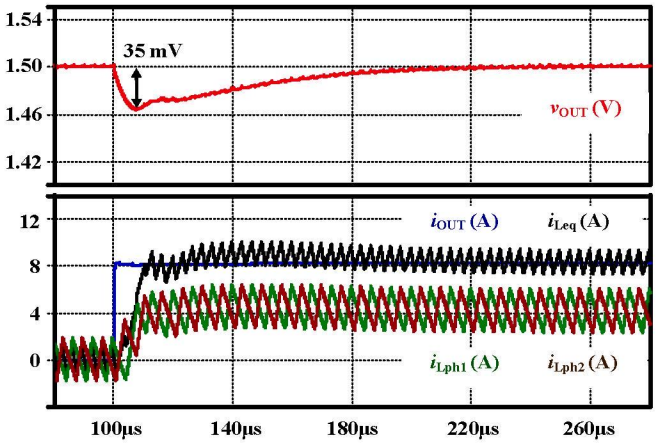

Figure 11. Simulation results – the load step-up Prototype B: C_{OUT} 2mF.

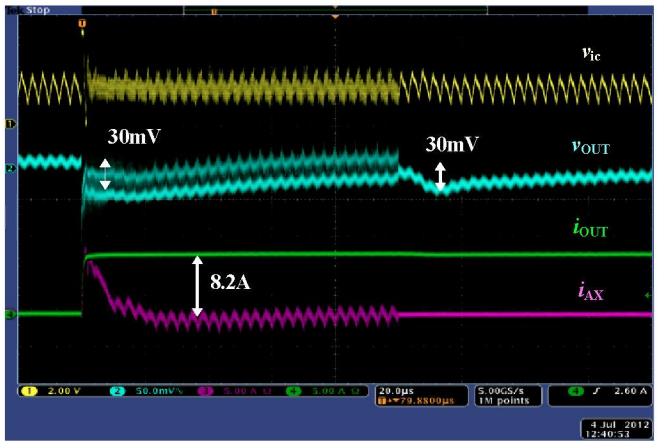

Figure 12. Experimental results – the load step-up Prototype A with the OICC: the load current i_{OUT} (green 5A/div), the auxiliary current i_{AX} (pink 5A/div), the output voltage v_{OUT} (blue 50mV/div), measured capacitor current v_{Ic} (yellow 2 V/div) and time 20µs/div.

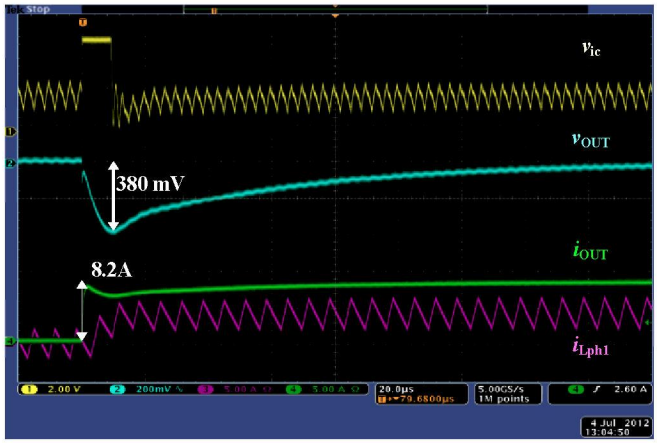

Figure 13. Experimental results – the load step-up Prototype A without the OICC: the load current i_{OUT} (green 5A/div), the first phase current i_{Lph1} (pink 5A/div), the output voltage v_{OUT} (blue 200mV/div), measured capacitor current v_{Ic} (yellow 2 V/div) and time 20µs/div.

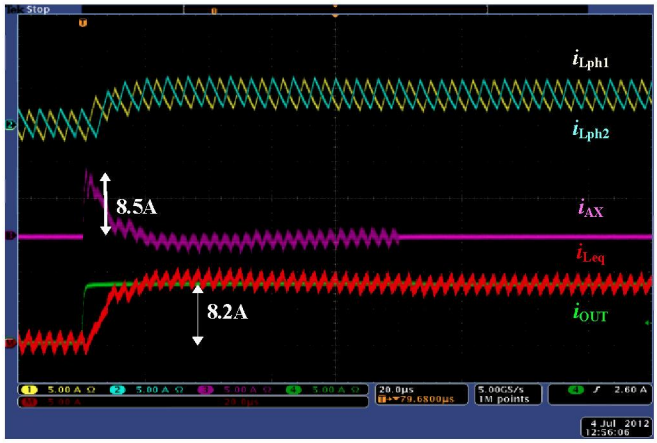

Figure 14. Experimental results – the load step-up Prototype A with the OICC: the load current i_{OUT} (green 5A/div), the auxiliary current i_{AX} (pink 5A/div), the first phase current i_{Lph1} (yellow 5A/div), the second phase current i_{Lph2} (blue 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div) and time 20µs/div.

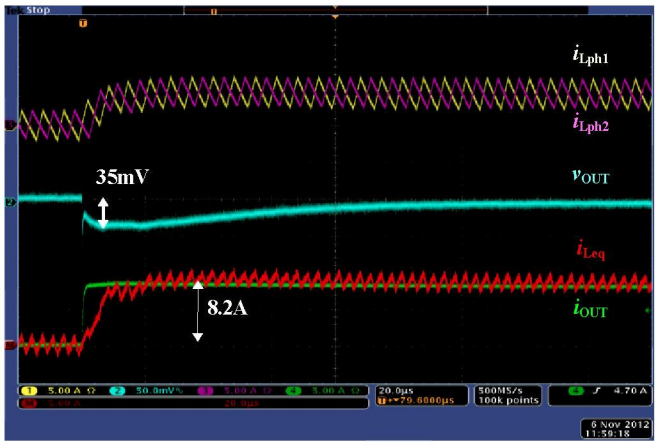

Figure 15. Experimental results – the load step-up Prototype B: the load current i_{OUT} (green 5A/div), the output voltage v_{OUT} (blue 50 mV/div), the first phase current i_{Lph1} (yellow 5A/div), the second phase current i_{Lph2} (pink 5A/div), sum of the first and second phase current i_{Leq} (red 5A/div) and time 20µs/div.

TABLE II. THE OUTPUT VOLTAGE DEVIATION

	Load step-up		**Load step-down**	
	simulation	***experiment***	***simulation***	***experiment***
Prototype A	-375 mV	-380 mV	500 mV	520 mV
Prototype A + OICC	-30 mV	-30 mV	45 mV	45 mV
Prototype B	-35 mV	-35 mV	40 mV	45 mV

technology to reduce the parasitic inductance of the vias that are connecting the output capacitor with the ground. Fig. 14 presents all the currents in Prototype A system. It can be seen how the auxiliary current (pink) is compensating the difference between the load current (green) and the sum of the phase currents (phase currents: yellow and blue; sum: red). Fig. 15 show all the system variables of Prototype B. Comparing the waveforms with corresponding ones of Fig. 12 and Fig. 14, it can be seen that both the output voltage v_{OUT} (see blue in Fig. 12 and blue in Fig. 15) and the sum of the phase currents i_{Leq} (see red in Fig. 14 and red in Fig. 15) have the same dynamic behavior in both systems.

The summary of the results for all three cases are presented in Table II and it can be seen that the experimental results are in a good agreement with the simulations.

Furthermore, by applying the OICC concept, the PCB area for the output capacitor has been reduced. The estimated area for the output capacitor for Prototype B, obtained by summing footprints areas of the capacitors, is 200.6 mm^2, while in the case of Prototype A, the estimated area is 92.8 mm^2, considering the footprints of output capacitors, the inductor, MOSFETs and the driver. As it is presented, the used area for the output capacitor and the OICC in discrete implementation is only 46% of the used area for Prototype B solution.

V. CONCLUSIONS

In this paper the Output Impedance Correction Circuit (OICC) concept is extended to Multiphase Current Controlled

Buck converter with PCMC. Various solutions can be employed to improve the dynamic behavior of the converter system, but nearly all solutions are developed for a Single Phase Buck converter with Voltage Mode Control (VMC), while in the VRM applications, due to the high currents, the system is usually implemented as a Multiphase Buck Converter with Current Mode Control. Due to the type of the control, the existing VMC solutions cannot be applied for systems with multiphase converters since current sharing cannot be ensured. As it is presented in this work, due to the control of all state variables, the OICC concept is extended to Multiphase solutions without significant modifications of the initial system presented in [18].

Furthermore, the OICC sub-system is implemented as a Synchronous Buck converter with PCMC providing better efficiency as a comparison to the solution based on the Linear Regulator, presented in [18]. In order to obtain that the auxiliary current, injected at the output node has the same value given by the auxiliary current reference voltage, the current ripple compensation block has been employed and implemented in a simple manner, thus obtaining good overlapping with real dependence of needed compensation voltage in certain range of the output voltage.

The system has been compared with a system which has n times bigger output capacitor. Two 2-phase Buck converter systems with PCMC have been designed, one with the OICC system which has multiplication factor 15 and another with 15 times bigger capacitor. Both systems exhibit the same dynamic behavior under the resistive load steps of 8.2 A at both simulation and experimental level, thus implying that the reduction of the output capacitor by factor 15 can be applied (from 2 mF to 140 μF). The prototypes have been built and tested under the same resistive load step and simulated results are in a good agreement with the experimental results: the output voltage deviation is -30 mV (-30 mV simulated) for positive load step for the system with OICC, while it is -380 mV (-375 mV simulated) for the system without the OICC. Similar results are obtained for the load step-down: 45 mV (45 mV simulated) and 520 mV (500 mV simulated) for the system with and without the OICC, respectively. In addition, the results of the second prototype with n times bigger capacitor present the same dynamic behavior as the first prototype which is employing the OICC: the output voltage deviation is -35 mV (-35 mV simulated and -30 for the OICC system) for positive load step, while it is 45 mV (40 mV simulated and 45 for the OICC system) for the load step-down. Furthermore, the reduction of the output capacitor area is obtained. The Prototype A solution uses 92.8 mm^2 (considering the footprints of output capacitors, the inductor, MOSFETs and the driver) for the output capacitor, while Prototype B uses 200.6 mm^2 (considering the footprints of output capacitors), thus the reduction to 46% of Prototype B solution has been obtained with the discrete implementation.